Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 80016

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2024
Third Semester
Electrical and Electronics Engineering
U23EE305 – DIGITAL LOGIC CIRCUITS
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q. No.	Questions	Marks	KL	CO
1.	Express the following unsigned decimal numbers in octal: 67.25, 12.	2	K2	CO1
2.	Work out the following additions using 1's complement signed representation: (the numbers are all expressed in hexadecimal) FA+8C, 7A+9B.	2	K2	CO1
3.	Represent A+B+C+D using only NAND gates.	2	K2	CO2
4.	Simplify the following using Boolean laws. $\overline{(\overline{AB} + \overline{AC} + \overline{BC})}$	2	K2	CO2
5.	Draw the combinational circuit for the full adder.	2	K2	CO3
6.	Interpret the operation of a binary-to-gray code converter using a truth-table for 4 bits.	2	K2	CO3
7.	What is the difference between latches and flip-flops?	2	K2	CO4
8.	Convert an SR latch to a JK flip-flop.	2	K2	CO4
9.	Consider a 4-bit ripple carry adder. Each full adder is implemented using a 3-input XOR gate, three 2-input AND gates and one 3-input OR gate. Consider the delay of each 3-input XOR gate to be 3 nanoseconds, the delay of each 2-input AND gate to be 1 nanosecond, and the delay of each 3-input OR gate to be 1 nanosecond. What will be the total time taken by the 4-bit ripple carry adder to perform a successful addition operation?	2	K3	CO5
10.	Mention few gate constructs used in gate level modelling.	2	K3	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Is A⊕ (B ⊕ C) = (A⊕ B) ⊕ C? Show that if A, B, and C are three binary variables that need to be added, the sum of the three is given by S = A ⊕ B ⊕ C, with a carry of C = AB + BC + CA.	13	K3	CO1
		(OR)			
	b)	If $\overline{A_3A_2A_1A_0}$ is a positive signed number, its 2's complement is given by $\overline{A_3A_2A_1A_0}$+ 0001. Prove that the above statement is true even if $\overline{A_3A_2A_1A_0}$ is a negative number.	13	K4	CO1
12.	a)	Consider the two functions: $f_1(A,B,C,D)$ = Π(1,3,5,11,15) $f_2(A,B,C,D)$ = Π(1,3,5,7,8,9,11) Express $f_3 = f_1 + f_2$ as a product of max-terms. Minimize the function $f_4 = f_1.f_2$ using a Karnaugh map.	13	K3	CO2
		(OR)			
	b)	Consider the design of a light for the staircase of a house. The light should be controlled from both the bottom and the top of the staircase. The rule to be followed is that switching either switch should change the state of the light, i.e, if the light was on it goes off, if it was off it goes on, when either switch is switched. Develop a truth table for this function.	13	K3	CO2
13.	a)	Design and describe a combinational circuit that generates the 9's complement of a BCD (binary-coded decimal) digit.	13	K3	CO3
		(OR)			
	b)	From the truth table find the combinational circuit to convert binary code to gray code.	13	K3	CO3
14.	a)	Design a mod 10 synchronous counter using JK flipflop.	13	K4	CO4
		(OR)			
	b)	Construct a 4-bit Johnson counter. List the eight unused states of the counter. Determine the next state for each of these states, and show that if the counter finds itself in an invalid state, it does not recover to a valid state.	13	K4	CO4
15.	a)	Explain about hazards & its elimination.	13	K2	CO5
		(OR)			
	b)	Design a synchronous modulo-7 counter. To design this, use a J-K flip-flop for the MSB, use a D-flip-flop for the middle bit, and use a T-flip-flop for the LSB. Show all design steps, including a state table, relevant Karnaugh maps, and your final circuit diagram.	13	K4	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Design a 4-bit ALU (Arithmetic Logical Unit) performing bitwise addition, subtraction, AND, OR, XOR and NAND operations with select-line.	15	K4	CO3
		(OR)			
	b)	Assume that every XOR gate has a propagation delay of 10 picosecond, and every AND or OR gate has a propagation delay of 5 picosecond. Draw a block diagram of a 16-bit carry-look-ahead type adder. How much time does the adder require to do one addition? Draw a block diagram of a 16-bit ripple-carry adder. How much time does the ripple-carry adder take to complete one addition?	15	K4	CO3